AMENDMENT TO THE DRAWINGS

Please replace the two drawing sheets showing Figs. 1a-1b and 2a-2b with the attached two "Replacement Sheet" drawing sheets showing Figs. 1a-1b and 2a-2b. Applicant submits that no new matter has been added.

Figs. 1a and 2a have been amended to remove reference number 30 and the lead line from reference No. 30. No new matter has been added to the drawings.

REMARKS

Upon entry of the above amendment, the drawing and the specification will have been amended. Additionally, claims 1, 10, 14, 16 and 21 will have been amended and claim 27 will have been added. Accordingly, claims 1-22 and 27 will be pending with claims 1, 16 and 27 being in independent form. Reconsideration of the Office Action and allowance of the present application and all the claims therein are respectfully requested and now believed to be appropriate.

Support for New Claim 27

Support for new claim 27 can be found in, e.g., original claim 1 and Figs. 1f and 2d. Applicant submits that no new matter has been added.

Objection to the Drawings

The drawings were objected to based on an informality. Applicant submits that the Examiner's objection to the drawings is moot with regard to the objection based on reference number 30 and improper and inconsistent with current USPTO rules with regard to the features recited in the claimed invention not being shown.

By this Amendment, Applicant has amended Figs. 1a and 2a to remove reference to reference number 30 so as to render this basis of objection moot.

Additionally, Applicant has reviewed the drawings and the claims consistent with the Examiner's comments. Applicant submits that each feature recited in the claims, e.g., claims 9 and 21, is fully described and sufficiently shown and/or illustrated in the drawings. Applicant further submits that one having ordinary skill in the art, having reviewed the specification and drawing, and having knowledge of the prior art relating to the invention, would have no difficulty understanding the invention recited in these claims.

Applicant submits, in particular, the drawing objection is improper because the features recited in the above-noted dependent claims are conventionally known and that one of ordinary skill in the art, having read the specification and viewed the drawings, would not require additional illustration to understand the features recited in the dependent claims. Current USPTO rules require drawings only "where necessary for the understanding of the subject matter sought to be patented" (see Rule 1.81(a)).

Applicant submits that on, e.g., the middle paragraph of page 10 of the specification, such features are acknowledged as being known. Because these features are conventionally known, no additional illustration is necessary or required. In conclusion, the features identified in the drawings in combination with what is know in the art, provide the ordinarily skilled artisan with sufficient illustration for the features recited in the above-noted claims consistent with current USPTO rules.

In view of the above, Applicant requests that the Examiner reconsider and withdraw

the objection to the drawings and indicate that the drawings are acceptable under current USPTO Rules.

Objection to the Specification

The specification was objected to based on an informality. Applicant submits that the Examiner's objection to the specification is moot. By this Amendment, Applicant has amended Figs. 1a and 2a to remove reference to reference number 30 so as to render this basis of objection moot.

In view of the above, Applicant requests that the Examiner reconsider and withdraw the objection to the specification and indicate that the specification is acceptable under current USPTO Rules.

Rejection under 35 U.S.C. Section 112, second paragraph

Claim 10 was rejected as being indefinite for containing a term which lacks proper antecedent basis. By this Amendment, Applicant has amended claim 10 so as to resolve the basis of this rejection. Specifically, the term "the Si layer" in claim 10 has been changed to "an Si layer".

In view of the above, Applicant requests that the Examiner reconsider and withdraw the objection to the specification and indicate that the specification is acceptable under current USPTO Rules.

Rejection Under 35 U.S.C. § 102(b)

Claims 1, 2, 4, 6, 7, 9, 10, 12, 16, 17 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. patent 6,399,970 to KUBO et al. This rejection is respectfully traversed.

Notwithstanding the Office Action assertions as to what KUBO discloses, Applicant submits that KUBO fails to disclose, or even suggest, for example, a first layer of material within the pFET channel having a lattice constant different than the lattice constant of the substrate, a second layer of material within the nFET channel having a lattice constant different than the lattice constant of the substrate, the second layer of material being different from the first layer of material, and an epitaxial semiconductor layer formed over the first layer of material in the pFET channel and the second layer of material in the nFET channel (claims 1 and 16). KUBO also does not disclose, or even suggest, the epitaxial semiconductor layer having substantially a same lattice constant as the substrate such that a stress component is created within the pFET channel and the nFET channel (claim 1) or the epitaxial semiconductor layer having substantially a same lattice constant as the substrate thus creating a stress component opposite to that of the first layer of material within the pFET channel and the second layer of material within the nFET channel (claim 16).

Applicant acknowledges that KUBO discloses a substrate 10 upon which pFET and NFET channels are formed. KUBO also discloses arranging layers 14n within the channels and that the "layer 14n and the Si layer 13n immediately therebelow are fitted in

lattice for each other" (see col. 8, lines 51-53). Finally, KUBO discloses, at col. 10, lines 51-57, "that the lattice misfit of the SiGeC layer 14n with respect to the Si substrate is zero ..." However, it is clear from a fair reading of KUBO that the various layers 14n/14p, 15n/15p, and 17n/17p in the nFET and pFET channels are of the same material. These layers are not different materials as recited in claims 1 and 16. For example, Fig. 1 of KUBO shows that both layers 14n and 14p in the pFET and nFET channels are SiGeC, that both layers 15n and 15p in the pFET and nFET channels are SiGe, and that layers 17n and 17p in the pFET and nFET channels are Si. KUBO also lacks any disclosure with regard to the use of different material layers in the channels in combination with an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel to create a stress component.

Thus, Applicant submits that the above-noted claims are not disclosed, or even suggested, by any proper reading of KUBO.

Furthermore, Applicant submits that dependent claims 2, 4, 6, 7, 9, 10, 12, 17 and 21 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicant submits that no proper reading of KUBO discloses or even suggests, in combination:

(i) a first layer of Si:C;

(ii) a Ge content of greater than 25%; and

(iii) a stress component of greater than 3 GPa.

Applicant respectfully requests that the rejection of the above-noted claims be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Claims 3, 11, 18 and 22 were rejected under 35 U.S.C. § 103(a) as unpatentable over KUBO in view of U.S. patent 6,790,699 to VOSSENBERG et al. Claims 5, 13 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over KUBO alone. Claims 8, 19 and 20 were rejected under 35 U.S.C. § 103(a) as unpatentable over KUBO in view of U.S. patent 5,683,934 to CANDELARIA. Claim 14 was rejected under 35 U.S.C. § 103(a) as unpatentable over KUBO in view of pages 256-257 of Silicon Processing for the Vlsi Era, Vol. 1: Process Technology, Second Edition, by Stanely WOLF et al.

The Examiner acknowledged that KUBO lacks, among other things, the separate forming of the pFET and nFET channels, the recited tensile stress value, a first layer of material that is Si:C, and a substrate that is silicon on insulator. However, the Examiner asserted that VOSSENBERG discloses the separate forming of the channels, that the recited tensile stress values would have been obvious on the basis of the teachings of KUBO alone. The Examiner further asserts that CANDELARIA teaches the use of carbon-doped silicon channel within a p-channel, and that WOLF teaches the silicon on insulator substrate. The Examiner also concludes that it would have been obvious to modify KUBO so as to render the features recited in the above-noted claims obvious to one of ordinary skill in the art. Applicant respectfully traverses each of the above-noted

rejections.

Applicant notes that VOSSENBERG merely discloses the manuafucturing process for a sensor using surface micromachining (see col. 3, lines 36-41). VOSSENBERG, however, lacks any disclosure with regard to the use of different material layers in pFET and nFET channels, much less, in combination with an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel. The Examiner has not identified any language in VOSSENBERG which discloses of suggests this feature.

Applicant notes that CANDELARIA merely discloses a channel layer 12 which comprises carbon-doped silicon (see col. 3, lines 45-50). CANDELARIA, however, does not disclose or suggest the features recited in 8, 19 and 20 in combination with the features recited in claims 1 and 16. Indeed, CANDELARIA specifically lacks any disclosure with regard to the use of different material layers in pFET and nFET channels, much less, in combination with an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel (claims 1 and 16). The Examiner has not identified any language in CANDELARIA which discloses of suggests these features.

Applicant notes that WOLF merely discloses that "[s]ilicon on insulator technology has been available since the late 1960's" (see page 256). WOLF, however, does not disclose or suggest the features recited in claim 14 in combination with the features recited in claim 1. Indeed, WOLF specifically lacks any disclosure with regard

to the use of different material layers in pFET and nFET channels, much less, in combination with an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel. The Examiner has not identified any language in WOLF which discloses of suggests this feature.

Additionally, Applicant submits that there is no motivation to modify KUBO in view of VOSSENBERG, CANDELARIA, and WOLF or in a manner which would render obvious Applicant's invention, and additionally, Applicant submits that there is no motivation or rationale disclosed or suggested in the prior art to modify the applied references in the manner suggested by the Examiner.

Applicant submits that dependent claims 3, 5, 8, 11, 13-15, 18-20 and 22 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicant submits that no proper combination of KUBO, VOSSENBERG, CANDELARIA, and WOLF discloses or even suggests, in combination:

the features recited in claims 3, 5, 8, 11 and 13-15 in combination with the features recited in claim 1 such as:

(i) the separate forming of the pFET and nFET channels;

(ii) the tensile stress in the epitaxial semiconductor layer being greater than 3 GPa;

(iii) the Si:C first layer;

(iv) forming the first and second layers with a hard mask over the pFET and nFET channels;

(v) the first and second layer heights of between about 100 Å and 300 Å;

(vi) the silicon on insulator; and

(vii) the Ge percentage of between 25% and 30%.

the features recited in claims 18-20 in combination with the features recited in claim 16 such as:

(i) the separate forming of the pFET and nFET channels;

(ii) the Si:C first layer and the SiGe second layer; and

(iii) the compressive stress in the pFET channel and the tensile stress in the nFET channel.

Applicant respectfully requests that the rejection of the above-noted claims be withdrawn.

New Claim is also Allowable

Applicant submits that the new claim 27 is allowable over the applied art of record. Specifically, claim 27 recites a combination of features which are clearly not disclosed or suggested by the applied art of record. Specifically, Applicant submits that the applied

documents fail to disclose or suggest, for example, providing a layer of Si:C within the pFET channel having a lattice constant different than the lattice constant of the substrate, providing a layer of SiGe within the nFET channel having a lattice constant different than the lattice constant of the substrate, and forming an epitaxial semiconductor layer over the layers of Si:C and SiGe in the pFET and the nFET channels.

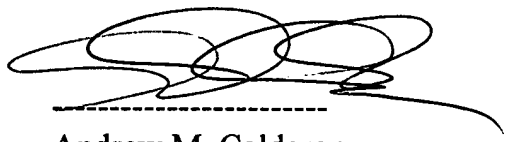
Accordingly, Applicant respectfully requests consideration of this claim and further request that the above-noted claim be indicated as being allowable.

CONCLUSION

In view of the foregoing, it is submitted that none of the references of record, either taken alone or in any proper combination thereof, anticipate or render obvious the Applicant's invention, as recited in each of the pending claims. The applied references of record have been discussed and distinguished, while significant claimed features of the present invention have been pointed out. Further, any amendments to the claims which have been made in this response and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto. Accordingly, reconsideration of the outstanding Office Action and allowance of the present application and all the claims therein are respectfully requested and now believed

to be appropriate. Authorization is hereby given to refund excess payments and charge any additional fee necessary to have this paper entered to Deposit Account No. 09-0458.

Respectfully submitted,
D. CHIDAMBARRAO et al.



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